Remarks

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

The specification and abstract have been reviewed and revised to make a number of editorial revisions. A substitute specification and abstract have been prepared and are submitted herewith. No new matter has been added. Enclosed is a marked-up copy of the original specification and abstract indicating the changes incorporated therein.

Figures 4 and 6 have been objected to as not being labeled as "Prior Art." Figures 4 and 6 have been amended so as to be labeled as "Prior Art." Substitute formal drawings are enclosed herewith including the changes to Figures 4 and 6. No new matter has been added. As a result, withdrawal of the objection to the drawings is respectfully requested.

The disclosure has been objected to as referring to Figures 4 and 6 as "conventional" while the figures themselves were not labeled as such. Figures 4 and 6 have now been labeled as "Prior Art." As a result, withdrawal of this objection is respectfully requested.

Claims 1-4 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chuang (US 6,003,151) in view of Sawada (US 6,600,779).

Claim 1-4 have been amended so as to further clarify the present invention from the references relied upon in the rejection.

In addition, claims 1-4 have been amended to make a number of editorial revisions. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, nor to address issues related to patentability and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

It is submitted that the above-mentioned rejection is no longer applicable to the claimed invention for the following reasons.

Claim 1 is patentable over the combination of Chuang and Sawada, since claim 1 recites a single processor having, in part, a descrambling/error detection block operable to read data after error correction from a first memory, descramble the data which has been subjected to the error correction, detect errors in the data after the descrambling, and thereafter store the data in a second memory.

The combination of Chuang and Sawada fails to disclose or suggest a descrambling/error detection block, as recited in claim 1.

Chuang discloses an error correction and detection system for a mass storage device. In a first embodiment of the error correction and detection system, a data string is received from an optical storage disk and converted into a form compatible with storage in a digital memory. The data string is then stored in a buffer while being provided to an error detection circuit. The error detection is performed on the data string to determine if any errors are present, with the error detection being performed while at least a portion of the data string is being stored in the buffer. If no errors are detected, the data string is transferred to a host computer. On the other hand, if errors are detected, then error correction is performed on the data string prior to the data string being transferred to the host computer. (See column 3, lines 42-65).

In a second embodiment of the error correction and detection system, a data string is received from an optical storage disk and stored in a buffer. The data string is then provided to a first error detection circuit where a first error detection is performed on the data string to determine a first error detection value characteristic of present errors. Error correction is performed on the data string to identify a first error in the data string and to determine an error pattern for the first error. The first error is then corrected in the data string and a second error detection is performed to determine if any errors remain in the data string. (See column 3, line 66 - column 4, line 19).

Based on the above discussion of the first and second embodiments of the error correction and detection system, it is apparent that Chuang generally discloses converting a data string into a form compatible with storage in a digital memory, error detection and error correction. However, it is apparent that Chuang fails to disclose or suggest a descrambling/error detection block operable to read data after error correction from a first memory, descramble the data which has been subject to the error correction, detect errors in the data after the descrambling, and thereafter store the data in a second memory. There is no disclosure of descrambling data which has been subject to error correction in Chuang.

As for Sawada, it discloses a signal processor for processing a read signal which utilizes a feedback loop for correcting errors in the read signal. In the combination, Sawada is relied upon as disclosing several methods of using a controller to control the error correction performance of the

signal processor. (See column 7, line 14 - column 8, line 19). However, it is apparent that Sawada, like Chuang, fails to disclose or suggest a descrambling/error detection block as recited in claim 1. As a result, the combination of Chuang and Sawada fails to disclose or suggest the present invention as recited in claim 1.

Because of the above mentioned distinctions, it is believed clear that claims 1-4 are patentable over the combination of Chuang and Sawada. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-4. Therefore, it is submitted that claims 1-4 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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DESCRIPTION

SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS

TECHNICAL FIELD

The present invention relates to a signal processor for detecting and correcting errors in data read from a recording medium.

BACKGROUND ART

In recent years, high quality and high speed ~~speedup~~ are demanded of a DVD-ROM, which has become widespread as a digital memory, to increase the reliability of data read from a DVD disk. With the demand, a signal processor for correcting errors in the disk is required to have rapid processing means, and it is aimed at realization of high-speed data processing.

A conventional CD-ROM signal processor performs error correction by a predetermined number of times. Further, the CD-ROM signal processor writes inputted data in a buffer memory and, simultaneously, detects errors in the data by using CRC (Cyclic Redundancy Check). Based on the result of CRC, when the data is decided as "error-free data", the signal processor reduces the predetermined number of error corrections.

In the case of DVD-ROM data, however, since inputted data is not previously subjected to error correction in contrast to the CD-ROM data, the error rate is higher in the DVD-ROM data than in the CD-ROM data. Therefore, when the DVD-ROM data is subjected to CRC, the result of CRC is, in most cases, that there are errors in the DVD-ROM data.

Figure 6 is a block diagram illustrating the structure of a conventional DVD-ROM signal processor.

In ~~figure~~ Figure 6, a DVD-ROM signal processor 65 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 61, and outputs the data after error correction to a host computer 63. The DVD-ROM signal processor 65 is under control of a control microcomputer 62, and is connected with a buffer memory 64 which stores data.

To be specific, the DVD-ROM signal processor 65 is provided with an FMT block 651 for capturing the DVD-ROM data outputted from the optical pickup 61, and storing it in the buffer memory 64; an error correction block 652 for correcting errors in the data stored in the buffer memory 64; a descrambling block 653 for descrambling the scrambled data; an error detection block 654 for detecting errors in the data after error correction, which data is stored in the buffer memory 64; a host interface block 655 for transmitting error-free data to the host computer, based on the result of the error detection by the error detection block 654; and a memory interface block 656 for controlling the processing between the DVD-ROM signal processor 65 and the buffer memory 64.

The operation of the conventional DVD-ROM signal processor so constructed will be described with reference to ~~figures~~ Figures 4 and 6.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in ~~figure~~ Figure 4, the logical format of the DVD-ROM data outputted from the optical pickup 61 is constituted with 182×208 bytes as one ECC (Error Correcting Code) block.

First of all, the data read by the optical pickup 61 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word comprising 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

In ~~figure~~ Figure 6, the FMT block 651 converts the DVD-ROM serial data outputted from the optical pickup 61 into parallel data (serial to parallel conversion), subjects the converted data to demodulation and sync detection, and writes the parallel data in the buffer memory 64 through the memory interface block 656.

The error correction block 652 reads the DVD-ROM data written in the buffer memory 64, through the memory interface block 656, performs syndrome calculation on the C1 code words and the C2 code words shown in ~~figure~~ Figure 4, and calculates the error position and the error pattern by using the result of the syndrome calculation. Based on the result of the syndrome calculation, the error correction block 652 terminates the error correction when the data has no error. However, when the data has some error, the error correction block 652 reads the error data stored in the buffer memory 64, through the memory interface block 656, performs error correction on the error data, and writes the corrected data over the address of the error data stored in the buffer memory 64, through the memory interface block 656.

The descrambling block 653 reads the DVD-ROM data which has been subjected to error correction and is stored in the buffer memory 64, through the

memory interface block 656, descrambles the data according to a predetermined method, and writes the data in the buffer memory 64 through the memory interface block 656.

The error detection block 654 reads the DVD-ROM data which has been descrambled and is stored in the buffer memory 64, through the memory interface block 656, and detects errors in the read data by performing a predetermined calculation.

The host interface block 655 transmits, to the host computer 63, the DVD-ROM data which has been decided as "error-free data" in both of the error correction block 652 and the error detection block 654.

Each of the above-mentioned blocks is constructed so as to operate at a predetermined timing according to an instruction from the control microcomputer 62.

In the conventional DVD-ROM signal processor, however, when the DVD-ROM data is subjected to error correction, the following operations are performed on the buffer memory 64: writing of data from the FMT block 651, reading and writing of data from the error correction block 652, reading and writing of data from the descrambling block 653, reading of data from the error detection block 654, and reading of data from the host interface block 655. That is, since reading and writing of data are performed frequently through the buffer memory 64, the memory band width is pressed and, therefore, the signal processor cannot perform high-speed access and higher-speed data processing.

The present invention is made to solve the above-described problem, and it is an object of the present invention to provide a signal processor which can reduce the number of memory accesses by reducing the number of error

corrections, thereby realizing higher-speed data processing.

SUMMARY ~~DISCLOSURE~~ OF THE INVENTION

A signal processor according to a first aspect of the present invention ~~(Claim 1)~~ is a signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block. This signal processor comprises: memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing; error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block; descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

In the signal processor so constructed, the number of data error corrections can be reduced, whereby reduced power consumption of the device itself can be achieved. Further, since the number of memory accesses to the memory means for error correction can be reduced, the access right to the memory means can be assigned to another block, whereby high-speed processing of the signal processor is realized.

According to the present invention ~~(Claim 2)~~, in the signal processor described in the first aspect ~~Claim 1~~, the error correction means comprises: a

syndrome calculator for calculating a syndrome of the data which has been subjected to the predetermined digital signal processing; an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation; error correction result holding means for holding information as to whether or not the data detected by the error position/pattern calculator is error-correctable ~~or not~~; data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and number-of-error-correction control means for controlling the number of error corrections.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by reducing the number of error corrections and, furthermore, speedup of data processing is achieved.

According to the present invention ~~(Claim 3)~~, in the signal processor described in the first aspect ~~Claim 1~~, the descrambling/error detection means comprises: descrambling means for descrambling the data which has been corrected by the error correction means; error detection means for detecting errors in the descrambled data; and error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

In the signal processor so constructed, based on the result of error detection, when there is no error, the data is transmitted to the host computer without performing error correction again, whereby the number of error corrections can be reduced. Accordingly, the power consumption of the device itself can be reduced.

According to the present invention ~~(Claim 4)~~, in the signal processor described in the first aspect~~Claim 1~~, the data subjected to the predetermined

digital signal processing is read from the memory means for each predetermined error correction block, followed by error detection and error correction; when there is some error, the error is corrected by the error correction means for each predetermined error correction block; when there is no error, the data is transmitted to the display means for each predetermined error correction block.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by terminating the second and more error corrections or reducing the number of error corrections for the data in each predetermined error correction block stored in the memory means, and further high-speed transmission of the data to the host computer is achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the structure of a DVD-ROM signal processor according to a first embodiment of the present invention.

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

Figure 5 is a timing chart of memory access in DVD-ROM signal processing according to a fourth embodiment.

Figure 6 is a block diagram illustrating the structure of the conventional DVD-ROM signal processor.

BEST MODE TO EXECUTE THE INVENTION

Embodiment 1.

Figure 1 is a block diagram illustrating the structure of a DVD-ROM signal processor according to a first embodiment of the present invention.

In ~~figure~~ Figure 1, a DVD-ROM signal processor 15 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 11, and outputs the data after error correction to a host computer 13. The DVD-ROM signal processor 15 is controlled by a control microprocessor (controller) 12, and ~~it connects~~ the DVD-ROM signal processor 15 is connected to a cache memory 16 for storing the data and to a buffer memory 14 for storing the data stored in the cache memory 16.

To be specific, the DVD-ROM signal processor 15 is provided with an FMT block 151 for capturing the DVD-ROM data outputted from the optical pickup 11; an error correction block 152 for correcting errors in the data stored in the cache memory 16 and the buffer memory 14; a descrambling/error detection block 153 for descrambling the scrambled data, and detecting errors in the descrambled data; an error detection block 154 for detecting errors in the data which has been subjected to error correction and is stored in the buffer memory 14; a host interface block 155 for transmitting error-free data to the host computer 13, based on the result of error detection by the error detection block 154; a memory interface block B 156 for controlling the processing between the DVD-ROM signal processor 15 and the buffer memory 14; and a memory interface block A 157 for controlling the processing between the DVD-ROM signal processor 15 and the cache memory 16.

The operation of the signal processor so constructed will be described with reference to ~~figures~~ Figures 1 and 4.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in ~~figure~~ Figure 4, the logical format of the DVD-ROM data outputted from the optical pickup 11 is constituted with 182×208 bytes as one ECC block.

First of all, the data read by the optical pickup 11 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word having 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

Initially, with reference to ~~figure~~ Figure 1, the DVD-ROM data outputted from the optical pickup 11 is converted from serial data to parallel data (serial to parallel conversion) by the FMT block 151. The parallel data are subjected to demodulation and sync detection, and one of the parallel data is written in the cache memory through the memory 16 interface block A 157. At the same time, another ~~the other~~ one of the parallel data is transmitted for each ECC block to the error correction block 152, wherein it is subjected to error correction. The data which has been subjected to error correction by the error correction block 152 is written in the cache memory 16 through the memory interface block A 157.

Next, the data after error correction is read from the cache memory 16

through the memory interface block A 157, and the scrambled data is subjected to descrambling and error correction by the descrambling/error detection block 153, and the data is transmitted to the buffer memory 14 through the memory interface block B 156. At this time, when the descrambling/error detection block 153 detects some error in the data, error correction is carried out again by the error correction block 152.

The data which has been subjected to error correction by the error correction block 152 is inputted to the error detection block 154 through the buffer memory 14 and the memory interface block B 156, wherein error detection is carried out again. Based on the result of the error detection, only the data decided as "error-free data" is transmitted to the host computer 13 through the host interface block 155.

As described above, in the signal processor according to the first embodiment, the DVD-ROM data inputted to the signal processor is subjected to error detection and error correction for every ECC block. When the data has some error, the data is subjected to error correction for every ECC block. When the data has no error, the data is transmitted to the host computer 13 for every ECC block. Therefore, although in the conventional example error correction is carried out by a predetermined number of times, such wasteful correction work is avoided, and the number of error corrections is reduced. Accordingly, it is possible to reduce the power consumption of the device itself. Further, since the number of memory accesses to the buffer memory 14 for error correction is reduced, the access right to the buffer memory 14 can be assigned to another block, whereby speedup of the signal processor is realized.

Embodiment 2.

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

With reference to ~~figure~~ Figure 2, an error correction block 152 is provided with a syndrome calculator 1521 for performing syndrome calculation; a scrambling circuit 1522 for scrambling descrambled data; an error position/pattern calculation block 1523 for calculating ~~the~~ an error position in data and ~~the~~ an error pattern on the basis of the result from the syndrome calculator 1521, and detecting data having uncorrectable errors (hereinafter referred to as "error uncorrectable data"); an error correction result holding circuit 1524 for holding information as to whether there is error uncorrectable data or not, which is detected in the error position/pattern calculation block 1523; data correction circuit 1525 for correcting errors in the data according to the error position and the error pattern calculated from the syndrome by the error position/pattern calculation block 1523; and a number-of-error-correction control circuit 1526 for controlling the number of error corrections.

The operation of the error correction block so constructed will be described with reference to ~~figure~~ Figure 2.

Initially, in the above-described first embodiment, the DVD-ROM data transmitted to the error correction block 152 is inputted to the syndrome calculator 1521 for each ECC block, wherein the data is subjected to syndrome calculation. At this time, if there is some error at the point of time when 182 bytes of data equivalent to the C1 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

In the error position/pattern calculation block 1523, it is detected whether

or not there is any uncorrectable error ~~or not~~, and the information about the presence or absence of uncorrectable error is stored in the error correction result holding circuit 1524. The information about the presence or absence of uncorrectable error, which is stored in the error correction result holding circuit 1524, is output to the number-of-error-correction control circuit 1526.

On the other hand, the information about the error position and the error pattern calculated in the error position/pattern calculation block 1523 is transmitted to the data correction circuit 1525. The data correction circuit 1525 reads the data stored in the address indicated by the error position from the cache memory 16 through the memory interface block A 157, and performs error correction by using the error position and the error pattern calculated by the error position/pattern calculation block 1523. The data which has been subjected to error correction by the data correction circuit 1525 is written in the address indicating the error position which is stored in the cache memory, through the memory interface block A 157.

The data which has been subjected to the first error correction in this way is subjected to error detection in the descrambling/error detection block 153, and transmitted to the buffer memory 14 through the memory interface block B 156. At this time, when some error is detected in the descrambling/error detection block 153, error correction is again carried out in the error correction block 152. Hereinafter, this process will be described in more detail.

In ~~figure~~ Figure 2, the number-of-error-correction control circuit 1526 decides whether there is any error in the data stored in the buffer memory 14, on the basis of the information from the error correction result holding circuit 1524 and the descrambling/error detection block 153 shown in ~~figure~~ Figure 1.

Based on the result of the detection, when there is no error, the number-of-error-correction control circuit 1526 outputs the status of "free from error" to the control microcomputer 12. However, when there is some error in the data stored in the buffer memory 14, the number-of-error-correction control circuit 1526 outputs the status of "error" to the control microcomputer 12, and the syndrome calculator 1521 performs syndrome calculation again.

The syndrome calculator 1521 reads the data with the error stored in the buffer memory 14, through the memory interface block B 156. The read data is initially subjected to scrambling by the scrambling circuit 1522, and then converted to the data that can be subjected to syndrome calculation. The converted data is inputted to the syndrome calculator 1521 for each ECC block, and subjected to syndrome calculation. If there is some error at the point of time when 182 bytes of data equivalent to the C1 code word or 208 bytes of data equivalent to the C2 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

Next, the information about the calculated error position and error pattern is transmitted to the data correction circuit 1525. The data correction circuit 1525 reads the data in the address indicating the error position from the buffer memory 14 through the memory interface block B_156, and performs error correction by using the error position and the error pattern calculated by the error position/pattern calculation block 1523. Then, the data which have been subjected to error correction in the data error correction circuit 1525 is written in the address indicating the error position of the data stored in the buffer memory 14, through the memory interface block B_156.

As described above, in the signal processor according to the second embodiment, syndrome calculation is performed on the data of each ECC block unit, which is inputted to the error correction block 152, and then error correction is performed on the data of each ECC block unit according to the result of the calculation. Therefore, the number of error corrections can be reduced and, furthermore, the number of memory accesses to the memory means can be reduced. Accordingly, high-speed data processing can be achieved.

Embodiment 3.

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

In ~~figure~~ Figure 3, a descrambling/error detection block 153 is provided with a descrambling circuit 1531 for descrambling scrambled data; an error detection circuit 1532 for detecting errors in the descrambled data; and an error detection result holding circuit 1533 for holding the result of error detection (presence or absence of error) by the error detection circuit 1532.

The operation of the descrambling/error detection block so constructed will be described with reference to ~~figure~~ Figure 3.

Initially, the data which has been subjected to error correction in the error correction block 152 is inputted to the descrambling circuit 1531 from the cache memory 16 through the memory interface block A 157, and the data is descrambled according to a predetermined method. The descrambled data is transmitted to the error detection circuit 1532, wherein errors in the data are detected by a predetermined calculation. The data after the error detection is transmitted to the buffer memory 14 through the memory interface block B 156.

Further, information about the result of the error detection by the error detection circuit 1532 is latched in the error detection result holding circuit 1533, and then outputted to the number-of-error-correction control circuit 1526 (see ~~figure~~ Figure 2) in the error correction block 152.

As described above, in the signal processor according to the third embodiment, the inputted data is descrambled and then subjected to error detection. Based on the result of the error detection, when there is no error, the data is transmitted to the host computer without performing data correction again. Therefore, the number of error corrections can be reduced, resulting in reduced power consumption of the signal processor.

Embodiment 4.

Figure 5 is a timing chart of memory access of a DVD-ROM signal processor according to a fourth embodiment of the present invention.

First of all, each of codes shown in ~~figure~~ Figure 5 will be described.

N∼N+3 denote block numbers of blocks when the data inputted to the DVD-ROM signal processor is subjected to error correction for each ECC block.

Process 1 denotes the process from when the data inputted to the DVD-ROM signal processor is inputted to the cache memory 16 and the error correction block 152 through the FMT block 151 to when the first error correction is carried out.

Process 2 denotes the process of performing the second and further error correction in the error correction block 152 when the data has some error in Process 1.

Process 3 denotes the process of transmitting error-free data to the host computer 13 through the host interface block 155 when the data has no error.

The operation of the DVD-ROM signal processor so constructed will be described with respect to the timing of memory access, with reference to ~~figure~~ Figure 5.

In ~~figure~~ Figure 5, for example, the data corresponding to the Nth, (N+2)th, and (N+3)th blocks are constituted by the error-free or error correctable C1 code word while the data corresponding to the (N+1)th block includes the error uncorrectable C1 code word.

Initially, with respect to the data in the Nth, (N+2)th, and (N+3)th blocks, these data having no errors at the point of time when Process 1 is ended are stored in the buffer memory 14. In this case, Process 1 is not followed by Process 2 but followed by Process 3 wherein the error-free data are transmitted for each ECC block to the host computer 13.

On the other hand, with respect to the data in the (N+1)th block, since this data has an error at the point of time when Process 1 is ended, Process 1 is followed by Process 2 wherein the error data is corrected. Those blocks containing the data which are finally decided as "error-free error" are transmitted to the host computer 13 in Process 3.

As described above, according to the signal processor of this fourth embodiment, the DVD-ROM data inputted to the signal processor is processed for every ECC block from when capture of the data is started to when the data is transmitted to the host computer 13. Therefore, in the case where Process 1 is performed on the data corresponding to one ECC block and then Process 3 is performed without performing Process 2 because there is no error, the access time inside the signal processor can be reduced by one ECC block. Accordingly, high-speed transmission of the data to the host computer 13 is

realized.

APPLICABILITY IN INDISTORY

As described above, the signal processor according to the present invention can reduce the number of memory accesses by reducing the number of error corrections to process data at higher speed. Especially, it is suitable as a signal processor for which ~~speedup~~ high speed is demanded, such as a DVD-ROM.